

# HANCHEN YE

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## EDUCATION

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- **University of Illinois at Urbana-Champaign**  
*Ph.D. Candidate* in Electrical and Computer Engineering *Aug. 2019 - Present*
- **Fudan University**  
*M.E.* in Integrated Circuit Engineering *Sep. 2017 - Jun. 2019*  
*B.E.* in Microelectronic Science and Engineering *Sep. 2013 - Jun. 2017*
- **National University of Singapore**  
*Exchange Program* in Electrical and Computer Engineering *Aug. 2015 - Dec. 2015*

## WORK EXPERIENCES

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- **SiFive, Platform Engineering Department**  
*Compilers Intern* mentored by Dr. Andrew Lenharth *May. 2021 - Aug. 2021*
- **Xilinx, Research Labs**  
*Compiler Intern* mentored by Dr. Stephen Neuendorffer *Jun. 2020 - Aug. 2020*
- **University of Illinois at Urbana-Champaign**  
*Research Assistant* mentored by Prof. Deming Chen *Aug. 2019 - Present*
- **Fudan University, State Key Laboratory of ASIC and System**  
*Research Assistant* mentored by Prof. Gengsheng Chen *Sep. 2016 - Jun. 2019*

## SELECTED PROJECTS

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- **CIRCT: Circuit IR Compilers and Tools** *Jun. 2020 - Present*
  - The CIRCT open-source project is an effort looking to apply MLIR and the LLVM development methodology to the domain of hardware design tools;
  - Contributed to the FIRRTL, HW (Hardware), and SV (SystemVerilog) dialects to establish the core IR of hardware and enable a Chisel to SystemVerilog compilation flow;
  - Contributed a new FSM dialect to represent, optimize, and generate codes for finite-state machines;
  - Contributed to the Handshake and StaticLogic dialects to enable a High-Level Synthesis (HLS) flow, which is a compilation pipeline from high-level programs to gate-level circuits.
- **ScaleHLS: Scalable High-Level Synthesis through MLIR** *Apr. 2020 - May. 2021*
  - Proposed a hierarchical HLS representation and optimization methodology in MLIR;
  - Designed a transform and analysis library dedicated for HLS applications;
  - Designed an HLS C front-end and a synthesizable C/C++ emission back-end for MLIR.
- **A Novel Design Paradigm of DNN Accelerator** *Feb. 2020 - Mar. 2021*
  - Proposed a novel paradigm which can take advantage of both pipeline and generic architecture;
  - Proposed an efficient design space exploration algorithm to generate optimized DNN accelerators following the new paradigm.
- **Hybrid Spatial and Winograd DNN Accelerator on FPGA** *Jan. 2019 - Dec. 2019*
  - Proposed a hybrid Spatial and Winograd convolution architecture for DNN acceleration;
  - Designed a comprehensive tool for the performance and area estimation and the design space exploration for both edge and cloud FPGAs.

- **Musket: RISCv-based IoT Sensor-Hub on FPGA** *Apr. 2018 - Aug. 2018*  
 - Pruned and transplanted a RISCv core to an edge FPGA and established a low-power SoC;  
 - Ported an RTOS to manage sensors and the wireless connection between FPGA and smartphones;  
 - Won the outstanding award of the 2nd China College IC Competition.
- **Dynamic and Pipelined CNN Accelerator on FPGA** *Oct. 2017 - May 2018*  
 - Proposed a Dynamic Partial Reconfiguration (DPR) -based pipeline architecture to deploy large CNN accelerators on resource-limited FPGAs while maintaining a low overall latency.

## PUBLICATIONS

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- [1] **ScaleHLS: Scalable High-Level Synthesis through MLIR**  
**Hanchen Ye**, Cong Hao, Jianyi Cheng, Hyunmin Jeong, Jack Huang, Stephen Neuendorffer, and Deming Chen  
*arXiv Preprint*, 2021
- [2] **ScaleHLS: Achieving Scalable High-Level Synthesis through MLIR**  
**Hanchen Ye**, Cong Hao, Hyunmin Jeong, Jack Huang, and Deming Chen  
*Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) of ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2021
- [3] **Being-ahead: Benchmarking and Exploring Accelerators for Hardware-Efficient AI Deployment**  
 Xiaofan Zhang, **Hanchen Ye**, and Deming Chen  
*Workshop on Benchmarking Machine Learning Workloads on Emerging Hardware (MLBench) of Conference on Machine Learning and Systems (MLSys)*, 2021
- [4] **DNNE Explorer: A Framework for Modeling and Exploring a Novel Paradigm of FPGA-based DNN Accelerator**  
 Xiaofan Zhang\*, **Hanchen Ye\***, Junsong Wang, Yonghua Lin, JinJun Xiong, Wen-mei Hwu, and Deming Chen (\* equal contributors)  
*IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2020
- [5] **IDLA: An Instruction-based Adaptive CNN Accelerator**  
 Peng Gao, Zhize Huang, **Hanchen Ye**, and Gengsheng Chen  
*IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2020
- [6] **HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation**  
**Hanchen Ye**, Xiaofan Zhang, Zhize Huang, Gengsheng Chen, and Deming Chen  
*ACM/IEEE Design Automation Conference (DAC)*, 2020
- [7] **A Resource-Sharing & Pipelined Design Scheme for Dynamic Deployment of CNNs on FPGAs**  
**Hanchen Ye** and Gengsheng Chen  
*IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2018
- [8] **A Novel Pipeline Design Method Based on FPGA Dynamic Partial Reconfiguration Technology**  
 Gengsheng Chen, **Hanchen Ye**, Siyu Ni, and Chao Huang  
*China Patent CN108228966A*, 2017

## TALKS

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- **FSM (Finite-State Machine) Dialect in CIRCT**  
*Circuit IR Compilers and Tools (CIRCT) Open Meeting* *Aug. 2021*

- **ScaleHLS: Scalable High-Level Synthesis through MLIR**  
*Xilinx Adaptive Compute Clusters (XACC) Tech Talk series* Aug. 2021  
*University of California at Santa Cruz (UCSC) HSC Seminar* May 2021  
*Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE)* Apr. 2021
- **Handshake-based High-level Synthesis in CIRCT**  
*Open-Source Development Tools (OSDT) Open Meeting* Aug. 2020  
*Circuit IR Compilers and Tools (CIRCT) Open Meeting* Aug. 2020
- **HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation**  
*Design Automation Conference (DAC)* Jul. 2020
- **A Resource-Sharing and Pipelined Design Scheme for Dynamic Deployment of CNNs on FPGAs**  
*International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* Nov. 2018

## AWARDS AND SCHOLARSHIPS

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- DAC 2020 Young Fellow Jun. 2020
- Outstanding Graduates of Shanghai (Top 2%) Jun. 2019
- KLA-Tencor Scholarship at Fudan University (8 per year) Dec. 2018
- Outstanding Students at Fudan University (Top 15%) Oct. 2018
- Outstanding Award of the 2nd China College IC Competition (9 out of 900) Aug. 2018
- Xi-Yuan Research Scholarship at Fudan University May 2016
- Outstanding Students at Fudan University (Top 15%) Dec. 2015

## SELECTED COURSES

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- **CS 526:** Advanced Compiler Construction (A) Spring 2021
- **ECE 527:** System-On-Chip Design (A+) Fall 2020
- **ECE 549:** Computer Vision (A) Spring 2020
- **ECE 598 NSG:** Deep Learning in Hardware (A+) Fall 2019
- **ECE 598 MS:** Adv Memory & Storage Systems (A) Fall 2019

## TECHNICAL SKILLS

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**Programming Languages** Verilog HDL, C++, Python, Cuda, Tcl, etc.  
**Frameworks & Tools** Vivado, Vivado HLS, Vitis, PyTorch, LLVM, MLIR, L<sup>A</sup>T<sub>E</sub>X, etc.