HANCHEN YE

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EDUCATION

- **University of Illinois at Urbana-Champaign**
  Ph.D. Candidate in Electrical and Computer Engineering — *Aug. 2019 - Present*
- **Fudan University**
  M.E. in Integrated Circuit Engineering — *Sep. 2017 - Jun. 2019*
  B.E. in Microelectronic Science and Engineering — *Sep. 2013 - Jun. 2017*
- **National University of Singapore**
  Exchange Program in Electrical and Computer Engineering — *Aug. 2015 - Dec. 2015*

WORK EXPERIENCES

- **Intel, Research Labs**
  Research Intern mentored by Dr. Jin Yang — *May. 2022 - Aug. 2022*
- **SiFive, Platform Engineering Department**
  Compilers Intern mentored by Dr. Andrew Lenharth — *May. 2021 - Aug. 2021*
- **Xilinx, Research Labs**
  Compiler Intern mentored by Dr. Stephen Neuendorffer — *Jun. 2020 - Aug. 2020*
- **University of Illinois at Urbana-Champaign**
  Research Assistant mentored by Prof. Deming Chen — *Aug. 2019 - Present*
- **Fudan University, State Key Laboratory of ASIC and System**
  Research Assistant mentored by Prof. Gengsheng Chen — *Sep. 2016 - Jun. 2019*

PUBLICATIONS

[1] **Invited: ScaleHLS: a Scalable High-Level Synthesis Framework with Multi-level Transformations and Optimizations**
Hanchen Ye, HyeGang Jun, Hyunmin Jeong, Stephen Neuendorffer, and Deming Chen
ACM/IEEE Design Automation Conference (DAC), 2022

[2] **ScaleHLS: A New Scalable High-Level Synthesis Framework on Multi-Level Intermediate Representation**
Hanchen Ye, Cong Hao, Jianyi Cheng, Hyunmin Jeong, Jack Huang, Stephen Neuendorffer, and Deming Chen
IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2022

[3] **Being-ahead: Benchmarking and Exploring Accelerators for Hardware-Efficient AI Deployment**
Xiaofan Zhang, **Hanchen Ye**, and Deming Chen
Workshop on Benchmarking Machine Learning Workloads on Emerging Hardware (MLBench) of Conference on Machine Learning and Systems (MLSys), 2021

[4] **ScaleHLS: Achieving Scalable High-Level Synthesis through MLIR**
Hanchen Ye, Cong Hao, Hyunmin Jeong, Jack Huang, and Deming Chen
Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) of ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021

[5] **DNNExplorer: A Framework for Modeling and Exploring a Novel Paradigm of FPGA-based DNN Accelerator**
Xiaofan Zhang*, **Hanchen Ye***, Junsong Wang, Yonghua Lin, JinJun Xiong, Wen-mei Hwu, and Deming Chen (* equal contributors)
IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2020

[6] **IDLA: An Instruction-based Adaptive CNN Accelerator**
Peng Gao, Zhize Huang, **Hanchen Ye**, and Gengsheng Chen
IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2020

[7] **HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation**
Hanchen Ye, Xiaofan Zhang, Zhize Huang, Gengsheng Chen, and Deming Chen
ACM/IEEE Design Automation Conference (DAC), 2020

[8] **A Resource-Sharing & Pipelined Design Scheme for Dynamic Deployment of CNNs on FPGAs**
Hanchen Ye and Gengsheng Chen
IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018

[9] **A Novel Pipeline Design Method Based on FPGA Dynamic Partial Reconfiguration Technology**
Gengsheng Chen, **Hanchen Ye**, Siyu Ni, and Chao Huang
China Patent CN108228966A, 2017

SELECTED PROJECTS

- **PolyAIE: A Polyhedral Compiler for Xilinx ACAP** *Oct. 2021 - Present*
  - Map C/C++ programs to the AI-Engine (AIE) array and Programming Logic (PL) on Xilinx ACAP using Polyhedral compilation techniques in MLIR.

- **CIRCT: Circuit IR Compilers and Tools** *Jun. 2020 - Present*
  - The CIRCT open-source project is an effort looking to apply MLIR and the LLVM development methodology to the domain of hardware design tools;
  - Contributed to the FIRRTL, HW (Hardware), and SV (SystemVerilog) dialects to establish the core IR of hardware and enable a Chisel to SystemVerilog compilation flow;
  - Contributed a new FSM dialect to represent, optimize, and generate codes for finite-state machines;
  - Contributed to the Handshake and StaticLogic dialects to enable a High-Level Synthesis (HLS) flow, which is a compilation pipeline from high-level programs to gate-level circuits.

- **ScaleHLS: A Scalable High-Level Synthesis Framework on MLIR** *Apr. 2020 - Present*
  - Proposed and designed a hierarchical HLS representation and optimization methodology in MLIR;
  - Designed a transform and analysis library dedicated for HLS applications;
  - Designed an HLS C front-end and a synthesizable C/C++ emission back-end for MLIR.

- **A Novel Design Paradigm of DNN Accelerator** *Feb. 2020 - Mar. 2021*
  - Proposed a novel paradigm which can take advantage of both pipeline and generic architecture;
  - Proposed an efficient design space exploration algorithm to generate optimized DNN accelerators following the new paradigm.

- **Hybrid Spatial and Winograd DNN Accelerator on FPGA** *Jan. 2019 - Dec. 2019*
  - Proposed a hybrid Spatial and Winograd convolution architecture for DNN acceleration;
  - Designed a comprehensive tool for the performance and area estimation and the design space exploration for both edge and cloud FPGAs.

- **Musket: RISCV-based IoT Sensor-Hub on FPGA** *Apr. 2018 - Aug. 2018*
  - Pruned and transplanted a RISCV core to an edge FPGA and established a low-power SoC;

- Ported an RTOS to manage sensors and the wireless connection between FPGA and smartphones;
- Won the outstanding award of the 2nd China College IC Competition.

- **Dynamic and Pipelined CNN Accelerator on FPGA** *Oct. 2017 - May 2018*
  - Proposed a Dynamic Partial Reconfiguration (DPR) -based pipeline architecture to deploy large CNN accelerators on resource-limited FPGAs while maintaining a low overall latency.

TALKS

- **ScaleHLS: A Scalable High-Level Synthesis Framework on MLIR**
  International Symposium on High-Performance Computer Architecture (HPCA'22) *Apr. 2022*
  FPGA Workshop on Open-Source Source-to-Source Transformation for High-Level Synthesis (HLS) *Feb. 2022*
  UIUC CS Compiler Seminar *Nov. 2021*
  Accelerated AI Algorithms for Data-Driven Discovery (A3D3) Kick-off Meeting *Nov. 2021*
  UIUC ECE527 (System-On-Chip Design) Guest Lecture *Nov. 2021*
  Xilinx Adaptive Compute Clusters (XACC) Tech Talk Series *Aug. 2021*
  UCSC Hardware Systems Collective (HSC) Seminar *May 2021*
  ASPLOS Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) *Apr. 2021*

- **Compilers for Domain-Specific Accelerators**
  Gatech ECE6100/CS6290 (Advanced Computer Architecture) Guest Lecture *Dec. 2021*
  CCF Agile Hardware Development and Open-Source EDA Forum *Jun. 2021*

- **FSM (Finite-State Machine) Dialect in CIRCT**
  Circuit IR Compilers and Tools (CIRCT) Open Meeting *Aug. 2021*

- **Handshake-based High-Level Synthesis in CIRCT**
  Open-Source Development Tools (OSDT) Open Meeting *Aug. 2020*
  Circuit IR Compilers and Tools (CIRCT) Open Meeting *Aug. 2020*

- **HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation**
  UIUC Ph.D. Qualifying Exam *Oct. 2020*
  Design Automation Conference (DAC) *Jul. 2020*

- **A Resource-Sharing and Pipelined Design Scheme for Dynamic Deployment of CNNs on FPGAs**
  International Conference on Solid-State and Integrated Circuit Technology (ICSICT) *Nov. 2018*

PROFESSIONAL SERVICES

- **External Reviewer**
  IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM) *2022*
  ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA) *2020*

- **Program Committee**
  ASPLOS Workshop on Languages, Tools, and Techniques for Accelerator Design (LATTE) *2022*

- **Reviewer**
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) *2021*
  Springer Neural Processing Letters (NEPL) *2021*

AWARDS AND SCHOLARSHIPS

- ECE Rambus Fellowship at UIUC *May 2022*

- DAC 2022 Young Fellow *Apr. 2022*
- DAC 2020 Young Fellow *Jun. 2020*
- Outstanding Graduates of Shanghai (Top 2%) *Jun. 2019*
- KLA-Tencor Scholarship at Fudan University (8 per year) *Dec. 2018*
- Outstanding Students at Fudan University (Top 15%) *Oct. 2018*
- Outstanding Award of the 2nd China College IC Competition (9 out of 900) *Aug. 2018*
- Xi-Yuan Research Scholarship at Fudan University *May 2016*
- Outstanding Students at Fudan University (Top 15%) *Dec. 2015*

SELECTED COURSES

- **CS 526:** Advanced Compiler Construction (A) *Spring 2021*
- **ECE 527:** System-On-Chip Design (A+) *Fall 2020*
- **ECE 549:** Computer Vision (A) *Spring 2020*
- **ECE 598 NSG:** Deep Learning in Hardware (A+) *Fall 2019*
- **ECE 598 MS:** Adv Memory & Storage Systems (A) *Fall 2019*

TECHNICAL SKILLS

Programming Languages	Verilog HDL, C++, Python, Cuda, Tcl, etc.
Frameworks & Tools	Vivado, Vivado HLS, Vitis, PyTorch, LLVM, MLIR, LaTeX, etc.